CONNTEK

KTP112 Series

High Performance, Low Power
Digital Temperature Sensor IC

Technical Support
sales.global@conntek.com.cn

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Table of Contents

1 Product Features

- Operating power supply range: $1.8V$ to $5.5V$
- Temperature operating range: $-40^{\circ}C$ to $125^{\circ}C$
- Ultra-low standby current:
  - $5.1\mu A$, $1Hz$ conversion cycle
  - $200nA$ standby power consumption
- High accuracy maintained over the entire temperature range:
  - $\pm 0.5^{\circ}C$ from $-40^{\circ}C$ to $125^{\circ}C$
- Programmable temperature alarm function
- Compatible with SMBus and I^2C interfaces

2 Applications

- Medical thermometers
- Environmental monitoring and thermostats
- Server and PC temperature detection
- Asset tracking and cold supply chain
- Gas meters and heat meters
- Testing and measurement
- Thermocouple cold junction compensation

3 Product Overview

The KTP112 is a high-precision, low-power digital temperature sensor that can replace NTC/PTC thermistors and can be used for temperature measurement in communications, computers, consumer electronics, environmental, industrial, and instrumentation applications. The KTP112 provides an accuracy of $\pm 0.5^{\circ}C$ over a normal operating range of $-40^{\circ}C$ to $+125^{\circ}C$ and has good temperature linearity. The KTP112 operates over a voltage range of $1.8V$ to $5.5V$, with a maximum standby current of $5.1\mu A$ (temperature measurement frequency $1Hz$) across the entire operating range. The internal 16-bit ADC resolution is as low as $0.0078^{\circ}C$. The KTP112 is packaged in a DFN2×2-6L package with integrated SMBus and I^2C interfaces, supporting up to four slaves on the same bus with SMBus alarm function.

4 Functional Block Diagram

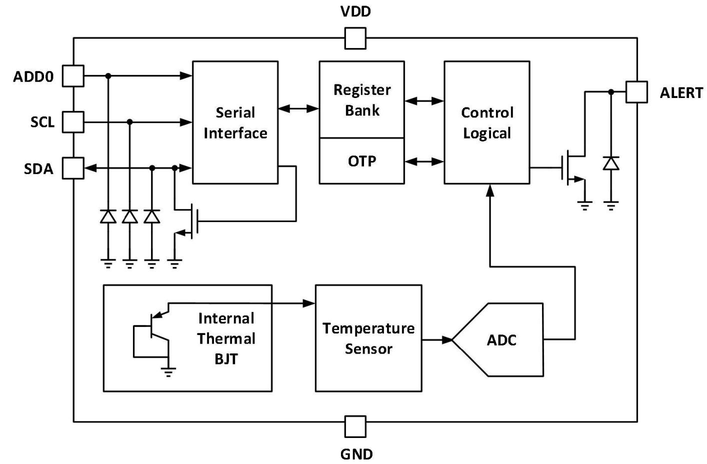


Figure 1: Functional Block Diagram of KTP112

5 Device Information

Part Number	Package	Package Size	Moisture Sensitivity Level
KTP112	DFN2×2-6L	$2.00mm \times 2.00mm$	MSL 3

6 Pin Out Information

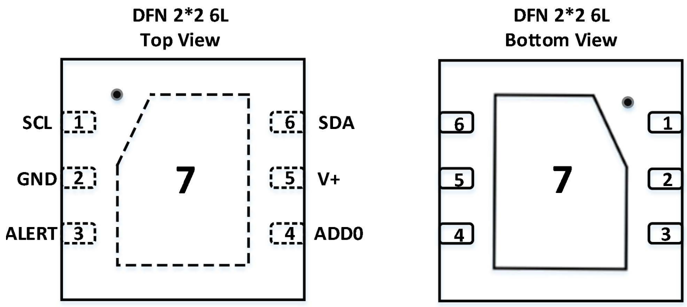


Figure 2: Pin Diagram of KTP112

Pin Name	Pin Number	Type	Description
SCL	1	I	Serial clock line; open-drain output; requires pull-up resistor
GND	2	-	Ground
ALERT	3	O	Over-temperature alarm output; open-drain output; requires pull-up resistor
ADD0	4	I	Address selection pin, can be connected to V+, GND, SCL, SDA
V+	5	I	Power supply input
SDA	6	I/O	Serial data line; open-drain output; requires pull-up resistor

7 Specifications

7.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min	Max
Power supply voltage, $V+$	-	$6V$
SCL, ADD0 and SDA voltage	$-0.3V$	$6V$
ALERT voltage	$-0.3V$	$((V+) + 0.3V)$, and $\leq 6V$
Operating junction temperature, T_J	-	$150^{\circ}C$
Storage temperature, T_{stg}	-	$150^{\circ}C$

7.2 ESD Ratings

Parameter	Value
ESD HBM (Human Body Model)	$\pm 2000V$
ESD CDM (Charged Device Model)	$\pm 500V$

7.3 Recommended Operating Conditions

Beyond the operating free-air temperature range (unless otherwise noted).

Symbol	Parameter	Min	Typical	Max
$V+$	Power supply voltage	$1.8V$	$3.3V$	$5.5V$
$V_{I/O}$	ALERT, SCL, ADD0, and SDA voltage	$0V$	$3.3V$	$5.5V$
T_A	Operating temperature	$-40^{\circ}C$	-	$125^{\circ}C$

7.4 Electrical Characteristics

Under the conditions of $T_A = +25°C$ and $V+ = 1.8V$ to $5.5V$, unless otherwise noted.

7.4.1 Digital Temperature Converter

Parameter	Test Conditions	Min	Typical	Max
Temperature range	-	$-40°C$	-	$125°C$
Temperature accuracy	$1Hz$ conversion cycle, thermal pad not connected (DFN package). $-40°C - 125°C$	-	$\pm 0.5°C$	$\pm 1°C$
DC power supply sensitivity	Single measurement mode, 8-sample average	-	$0.0156°C/V$	-
Temperature resolution (LSB)	-	-	$0.0078°C$	-
Reproducibility[1]	$V+ = 3.3V$, $1Hz$ conversion cycle	-	$\pm 2LSB$	-
Long-term stability and drift[2]	$150°C$, 1000 hours	-	$0.0156°C$	-
Temperature cycle and hysteresis[3]	8-sample average	-	$\pm 2LSB$	-
Conversion time	Single measurement mode	-	$124ms$	-

[1] Reproducibility is the ability to reproduce the reading when the same temperature is applied continuously under the same conditions. [2] Long-term drift is determined through an accelerated life test of 1000 hours at a junction temperature of $125°C$. [3] The definition of hysteresis here is the ability to reproduce the temperature reading during temperature changes from room temperature to hot, back to room temperature, to cold, and then back to room temperature. The temperatures used for this test are $-40°C$, $25°C$, and $125°C$.

7.4.2 Digital Input/Output

Parameter	Test Conditions	Min	Typical	Max
C_{IN}, input capacitance	-	-	2pF	-
V_{IH}, input logic high voltage	SCL, SDA	$0.7 \times (V+)$V	-	-
V_{IL}, input logic low voltage	SCL, SDA	-	-	$0.3 \times (V+)$V
I_{IN}, input leakage current	-	$-0.1\mu A$	-	$0.1\mu A$
V_{OL}, SDA and ALERT low-level output voltage	$I_{OL} = 10mA$	0V	-	0.4V
Resolution	-	-	16 Bits	-
Conversion mode	CR1=0, CR0=0	-	0.25 Conv/s	-
	CR1=0, CR0=1	-	1 Conv/s	-
	CR1=1, CR0=0 (default)	-	4 Conv/s	-
	CR1=1, CR0=1	-	8 Conv/s	-
Timeout	-	-	30ms	40ms

7.4.3 Power Supply

Parameter	Test Conditions	Min	Typical	Max
Operating voltage range	-	$1.8V$	$3.3V$	$5.5V$
I_{Q_ACTIVE}, quiescent current during conversion	Effective conversion, communication off	-	$13.5\mu A$	-
I_Q, quiescent current	1Hz working frequency, communication off, $T_A = 25°C$	-	$5.1\mu A$	-
I_{SB}, standby current[4]	Communication off	-	$3.9\mu A$	-
I_{SD}, shutdown current	Communication off	-	$0.2\mu A$	-
V_{POR}, power-on-reset voltage threshold	Power-up	-	$1.6V$	-
V_{PDD}, power-down detection	Power-down	-	$1.1V$	-
t_{RESET}, reset time	Time for device reset	-	$1.8ms$	-

[4] Standby current between conversions.

Within the free-air temperature range $T_A = -40°C$ to $125°C$, $V+ = 1.8V$ to $5.5V$, typical specifications at $T_A = +25°C$ and $V+ = 3.3V$ (unless otherwise noted).

7.5 Timing Requirements

Refer to the Timing Diagram Section:**??** for details on timing diagrams.

Parameter	Test Conditions	Fast Mode		High-Speed Mode		Unit
		Min	Max	Min	Max	
f_{SCL}, SCL clock frequency	V+	0.001	0.4	0.001	2.85	MHz
t_{BUF}, bus free time between a STOP and START condition	Refer to Fig. 7	600	-	160	-	ns
t_{HDSTA}, hold time after (repeated) START condition	Refer to Fig. 7	600	-	160	-	ns
t_{SUSTA}, setup time for a repeated START condition	Refer to Fig. 7	600	-	160	-	ns
t_{SUSTO}, setup time for STOP condition	Refer to Fig. 7	600	-	160	-	ns
t_{HDDAT}, data hold time	Refer to Fig. 7	100	900	25	105	ns
t_{SUDAT}, data setup time	Refer to Fig. 7	100	-	25	-	ns
t_{LOW}, SCL clock low voltage period	V+, Refer to Fig. 7	1300	-	210	-	ns
t_{HIGH}, SCL clock high voltage period	Refer to Fig. 7	600	-	60	-	ns
t_{FD}, data fall time	Refer to Fig. 7	-	300	-	80	ns
t_{RD}, data rise time	Refer to Fig. 7	-	300	-	-	ns
	$SCLK \leq 100$ kHz, refer to Fig. 7	-	1000	-	-	ns
t_{FC}, fall time of SCL signals	Refer to Fig. 7	-	300	-	40	ns
t_{RC}, rise time of SCL signals	Refer to Fig. 7	-	300	-	40	ns

7.6 Measurement Curves

Tested in an oil bath at $T_A = +25°C$, $V+ = +3.3V$, unless otherwise noted.

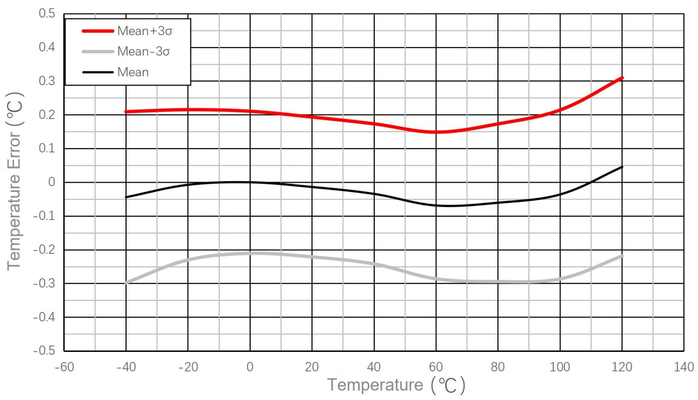


Figure 3: 1Hz Conversion Cycle, DFN Package, Temperature Error vs Temperature

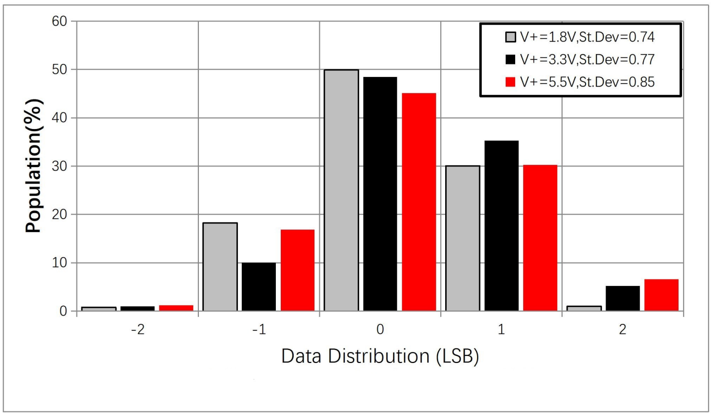


Figure 4: Data Distribution (LSB) vs Population (%)

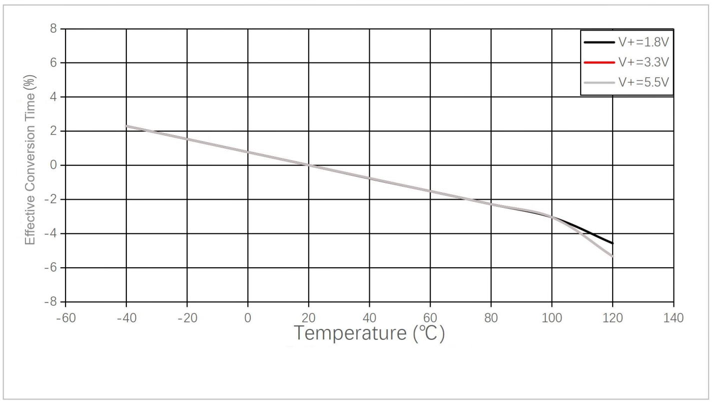


Figure 5: 25°C, $V+ = 3.3V$, Effective Conversion Time Variation Percentage vs Temperature

8 Detailed Description

8.1 Overview

The KTP112 series devices are digital temperature sensors best suited for thermal management and thermal protection applications. The KTP112 series is compatible with SMBus and I^2C interfaces. The operating temperature range is $-40°C$ to $125°C$. Figure 6 shows the block diagram of the KTP112 series.

The temperature sensor in the KTP112 series is the chip itself. The thermal path runs through the package leads and the plastic packaging. Due to the low thermal resistance of the metal, the package leads provide the primary thermal path.

8.2 Functional Block Diagram

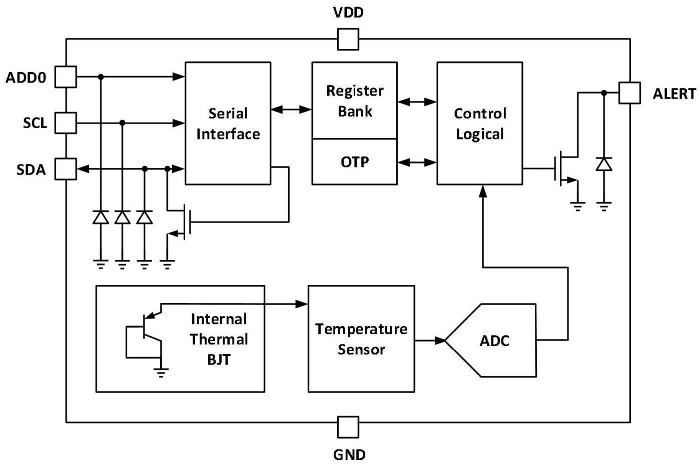


Figure 6: Functional Block Diagram

8.3 Functional Description

8.3.1 Power-Up

After the power supply voltage reaches the operating range, the device requires a $1.5ms$ power-up time before conversion starts, and it can be programmed to initiate power-up in shutdown mode. Before temperature conversion, the temperature register reads 0.

8.3.2 Temperature Result and Limits

At the end of each conversion, the result is updated in the temperature register. The data in the result register is in binary complement format, with a data width of 16 bits and a resolution of $7.8125m^{\circ}C$. Table 1 shows several examples of binary data that can be read from the temperature result register and the corresponding hexadecimal and temperature equivalents. The KTP112 series also has alarm status flags and an alert pin function, which use temperature limit values stored in the lower and upper limit registers. The data format of the temperature result register is used for writing data to the upper and lower limit registers.

Table 1: 16-bit Temperature Data Format of the values in the temperature register with the resolution of $7.8125m^{\circ}C$

Temperature ($^{\circ}C$)	Binary	Hexadecimal
-256	1000000000000000	8000
-25	1111001110000000	$F380$
-0.1250	1111111111110000	$FFF0$
-0.0078125	1111111111111111	$FFFF$
0	0000000000000000	0000
0.0078125	0000000000000001	0001
0.1250	0000000000010000	0010
1	0000000010000000	0080
25	0000110010000000	$0C80$
100	0011001000000000	3200
255.9921	0111111111111111	$7FFF$

8.3.3 Serial Interface

The KTP112 series operates only as a slave device on SMBus and I^2C interface-compatible buses. Integrated spike suppression filters and Schmitt triggers on the open-drain I/O lines, SDA and SCL pins, minimize input spikes and bus noise effects. The KTP112 series supports both Fast Mode (1kHz to 400kHz) and High-Speed Mode (1kHz to 2.85MHz) transfer protocols. All data bytes are transmitted MSB first.

8.3.4 Bus Overview

The device that initiates transmission is called the master, and the devices under the master's control are slaves. The bus must be controlled by a single master device that generates the serial clock (SCL), controls bus access, and generates start and stop conditions.

To address a specific device, a start condition is initiated by pulling the data line (SDA) from high to low when the SCL pin is high. All slave bits on the bus are at the rising edge of the clock. The last bit indicates whether a read or write operation is intended. On the ninth clock pulse, the addressed slave responds to the master by generating an acknowledgment and pulling the SDA pin low.

Data transmission is then initiated and sent over eight clock pulses followed by an acknowledgment bit. During data transmission, the SDA pin must remain stable while the SCL pin is high because any changes on the SDA pin while the SCL pin is high are interpreted as start or stop signals.

When all data has been transmitted, the master generates a STOP condition by pulling the SDA pin from low to high while the SCL pin is high.

8.3.5 Serial Bus Address

To communicate with a device, the master must first address it via a slave address byte. The slave address consists of seven address bits and a direction bit indicating the operation to be performed (read or write).

The KTP112 series has an address pin that allows addressing up to four devices on a single bus. Table 2 describes the logic levels for correctly connecting up to four devices.

Table 2: Address Pin and Slave Address

Two-Wire Address	ADD0 Pin Connection
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL

8.3.6 Read and Write Operations

Access to specific registers on the KTP112 series is accomplished by writing the pointer register to the appropriate value. The pointer register value is transmitted as the first byte after the slave address byte with the $R/\overline{W}$ bit low. Each write operation to the KTP112 series requires a pointer register value (see Figure 8).

When reading from the KTP112 series, the last value stored in the pointer register by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, the pointer register must be written to a new value. This operation is accomplished by issuing a slave address byte with the $R/\overline{W}$ bit low, followed by a pointer register byte. No additional data is required. The master can then generate a start condition and send the slave address byte with the $R/\overline{W}$ bit high to initiate the read command. See Figure 8 for more details on this sequence. If repeated reads from the same register are required, the pointer register value does not need to be sent continuously because the KTP112 series retains the pointer register value until the next write operation changes it.

Register bytes are sent MSB first, followed by LSB.

8.3.7 Slave Mode Operations

The KTP112 series can operate as a slave receiver or slave transmitter. As a slave device, the KTP112 series never drives the SCL line.

Slave Receiver Mode The first byte transmitted by the master is the slave address with the $R/\overline{W}$ bit low. The KTP112 series acknowledges receiving a valid address. The next byte transmitted by the master is the pointer register. The KTP112 series acknowledges receiving the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The KTP112 series acknowledges receiving each data byte. The master terminates data transfer by generating a start or stop condition.

Slave Transmitter Mode The first byte transmitted by the master is the slave address with the $R/\overline{W}$ bit high. The slave address is received, and a valid address is acknowledged. The next byte transmitted by the slave is the most significant byte of the register indicated by the pointer register. The master acknowledges receiving the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges receiving the data byte. The master can terminate data transfer by generating a start or stop condition or by not acknowledging the received data byte.

8.3.8 SMBus Alert Function

The KTP112 series supports the SMBus alert function. When the KTP112 series is in interrupt mode (TM=1), the alert pin can be connected as an SMBus alert signal. When the master senses an alert condition on the alert line, the master sends an SMBus alert command (00011001) to the bus. If the alert pin is active, the device acknowledges the SMBus alert command and responds by returning the slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates whether the alert condition was caused by a temperature exceeding T_{HIGH} or falling below T_{LOW}. If the temperature is greater than T_{HIGH}, the LSB is high; if the temperature is less than T_{LOW}, the LSB is low. For more details on this sequence, see Figure 10.

If multiple devices on the bus respond to the SMBus alert command, arbitration of the slave address portion of the SMBus alert command determines which device clears its alert status. The device with the lowest two-wire address wins the arbitration. If the KTP112 series wins the arbitration, the alert pin becomes inactive; if the KTP112 series loses the arbitration, the alert pin remains active.

8.3.9 General Call Response

The KTP112 series responds to a two-wire general call address (0000000) if the eighth bit is 0. The device acknowledges the general call address and responds to the command in the second byte. If the second byte is 00000110, the KTP112 series resets its internal registers to the power-on initial values. The KTP112 series does not support the general address acquire command.

8.3.10 High-Speed (HS) Mode

To enable two-wire bus operation above $400kHz$, the master device must issue an Hs-mode master code (0000 1xxx) as the first byte after a start condition to switch the bus to high-speed operation. The KTP112 series does not acknowledge this byte but switches the input and output filter on the SDA and SCL pins to operate in Hs-mode, allowing transfers up to $2.85MHz$. After the Hs-mode master code is issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a stop condition is generated on the bus. After a stop condition is received, the KTP112 series switches the input and output filters back to fast-mode operation.

8.3.11 Timeout Function

If the SCL pin is held low for $30ms$ (typical) between a start and stop condition, the KTP112 series resets the serial interface. If the SCL pin is held low and waits for a start condition from the master controller, the KTP112 series releases the SDA line. To avoid activating the timeout function, keep the SCL working frequency at least $1kHz$.

8.3.12 Timing Diagrams

The KTP112 series is compatible with SMBus and I^2C interfaces. Figures 7 to Figure 10 describe various operations on the KTP112 series. Parameters for Figure 7 are defined in the Timing Requirements section. The bus definitions are as follows:

- **Bus Idle**: Both SDA and SCL lines remain high.
- **Start Data Transfer**: A change in the state of the SDA line, from high to low, while the SCL line is high, defines a start condition. Each data transfer is initiated with a start condition.
- **Stop Data Transfer**: A change in the state of the SDA line, from low to high, while the SCL line is high, defines a stop condition. Each data transfer is terminated with a repeated start or stop condition.
- **Data Transfer**: The number of data bytes transferred between a start and stop condition is not limited and is determined by the master device. The KTP112 series can also be used for single-byte updates. To update only the MS byte, terminate the communication by issuing a start or stop condition on the bus.
- **Acknowledge**: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The master device must generate an extra clock pulse which is associated with this acknowledge bit. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by a not-acknowledge (1) for the last byte received.

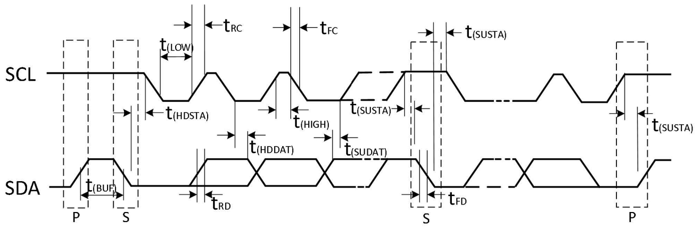


Figure 7: I^2C Timing Diagram

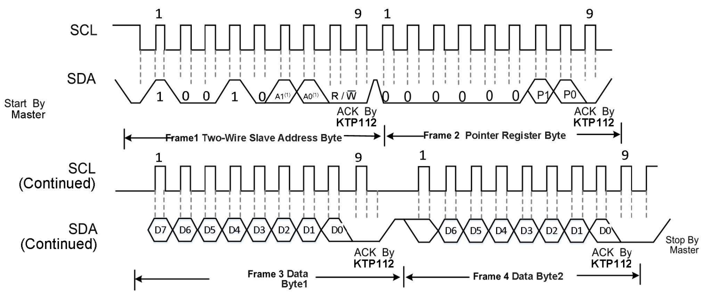


Figure 8: Write Register Timing Diagram

A0 and A1 are determined by the ADD0 pin.

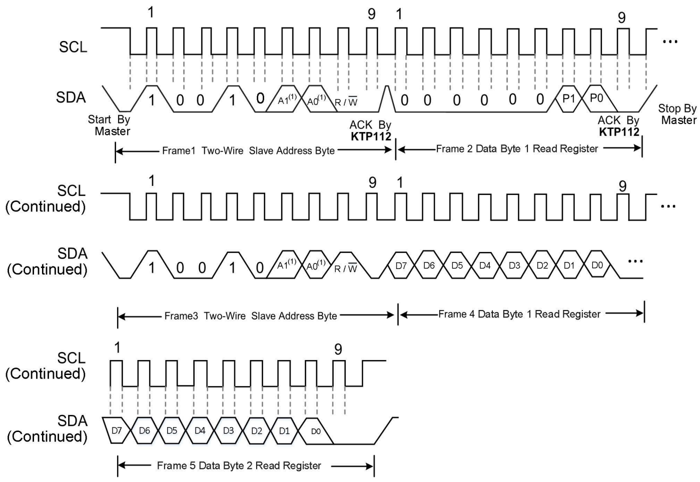


Figure 9: Read Register Timing Diagram

1) A0 and A1 are determined by the ADD0 pin. 2) The user should keep SDA high to terminate a single-byte read operation. 3) The user should keep SDA high to terminate a two-byte read operation.

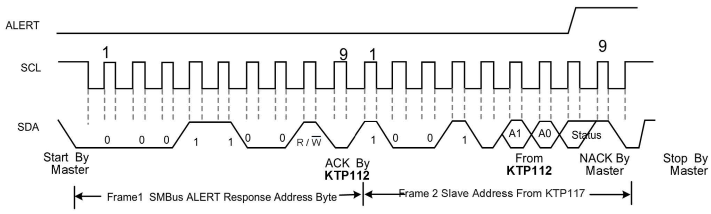


Figure 10: SMBus ALERT Timing Diagram

A0 and A1 are determined by the ADD0 pin.

8.4 Device Functional Modes

8.4.1 Continuous Conversion Mode

The default mode of the KTP112 series is continuous conversion mode. In continuous mode, the ADC performs continuous temperature conversions and stores each result in the temperature register, overwriting the previous result. The conversion rate bits, CR1 and CR0, configure the KTP112 series for conversion rates of $0.25Hz$, $1Hz$, $4Hz$, or $8Hz$. The typical conversion time for the KTP112 series is $124ms$. To achieve different conversion rates, the KTP112 series performs a conversion, powers down, and waits for the appropriate delay set by CR1 and CR0. Table 3 lists the CR1 and CR0 settings.

Table 3: Conversion Rate Settings

CR1	CR0	Conversion Rate
0	0	$0.25Hz$
0	1	$1Hz$
1	0	$4Hz$ (default)
1	1	$8Hz$

After power-up or a general reset, the KTP112 series begins conversions immediately, as shown in Figure 11. The first result is available after $124ms$ (typical). The active standby current during conversion is $13.7\mu A$ (typical at $27°C$). The standby current during the delay period is $3.9\mu A$ (typical at $27°C$).

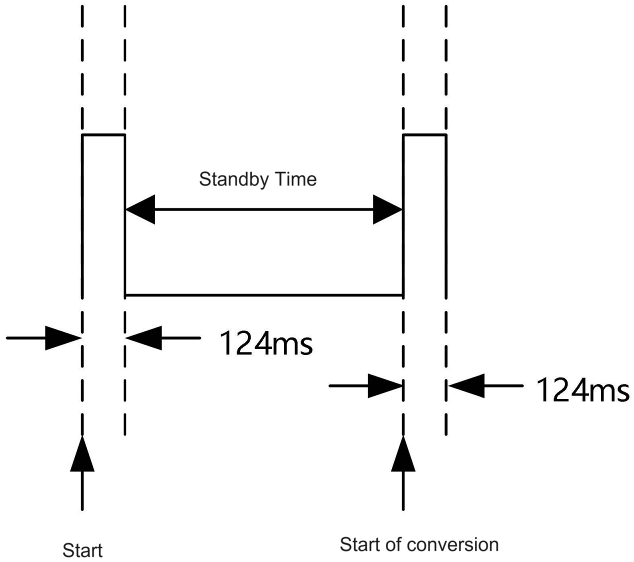


Figure 11: Conversion Start

Standby time is determined by CR1 and CR0.

The average power consumption of the device in continuous mode can be calculated using Equation below:

$$\text{Average Power Consumption} = \frac{\text{Active Power} \times \text{Active Conversion Time} + \text{Standby Power} \times \text{Standby Time}}{\text{Conversion Time Period}}$$

8.4.2 One-Shot/Conversion Ready Mode (OS)

The KTP112 series features a one-shot temperature measurement mode. When the device is in shutdown mode, writing a 1 to the OS bit initiates a single temperature conversion. During conversion, the OS bit reads 0. After the single conversion is completed, the device returns to shutdown mode. The OS bit reads 1 after conversion. This feature can be used to reduce the KTP112 series power consumption when continuous temperature monitoring is not required. Due to the short conversion time, the KTP112 series can achieve high conversion rates. A single conversion typically occurs in $124ms$, and a read can occur in less than $20\mu s$. Using one-shot mode, up to eight conversions per second can be achieved.

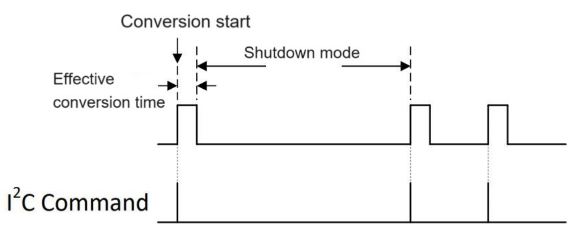


Figure 12: One-Shot Measurement Mode Timing Diagram

8.4.3 Thermostat Mode (TM)

The thermostat mode bit indicates whether the device operates in comparator mode (TM=0) or interrupt mode (TM=1).

8.4.4 Comparator Mode (TM=0)

In comparator mode (TM=0), the alert pin is activated when the temperature equals or exceeds the value in the T_{HIGH} register and remains active until the temperature falls below the value in the T_{LOW} register. For more information on comparator mode, see the upper and lower limit registers section.

8.4.5 Interrupt Mode (TM=1)

In interrupt mode (TM=1), the alert pin is active when the temperature exceeds the T_{HIGH} register or falls below the T_{LOW} register. The alert pin is cleared when the host controller reads the temperature register. For more information on interrupt mode, see the upper and lower limit registers section.

8.5 Configuration

8.5.1 Pointer Register

Figure 13 shows the internal register structure of the KTP112 series. The device uses an 8-bit pointer register to address a given data register. The pointer register uses the two LSBs to identify which data register must respond to a read or write command. The power-on reset value of P1/P0 is "00". By default, the KTP112 series reads the temperature register upon power-up.

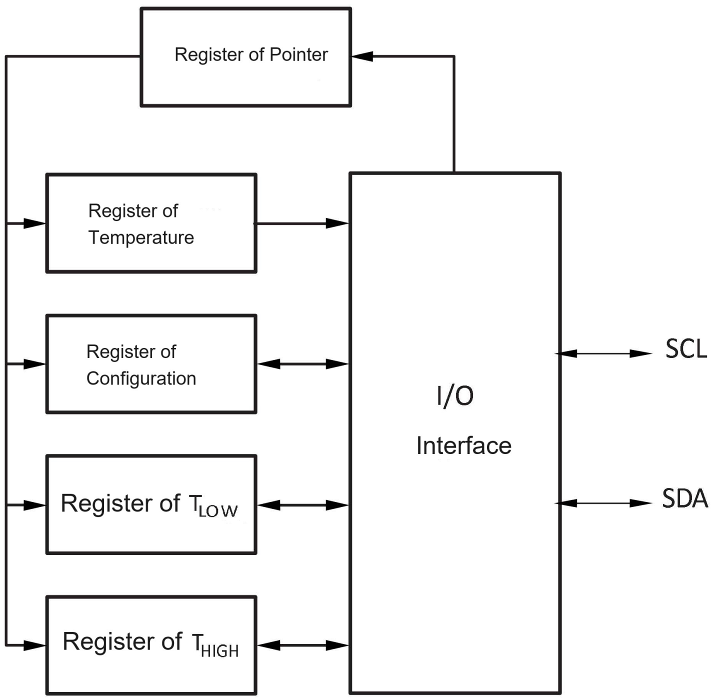


Figure 13: Internal Register Structure

Table 4 lists the pointer addresses of the available registers in the KTP112 series. Table 5 lists the bits of the pointer register byte. Bits P2 to P7 must always be 0 in write commands.

Table 4: Pointer Addresses

P1	P0	Register
0	0	Temperature Register (Read-only)
0	1	Configuration Register (Read/Write)
1	0	T_{LOW} Register (Read/Write)
1	1	T_{HIGH} Register (Read/Write)

Table 5: Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

8.5.2 Temperature Register

The temperature register in the KTP112 series is configured as a 16-bit read-only register that must be read as two bytes to obtain data, as shown in Tables 6 and Figure 7. The 16-bit data with sign bits is used to indicate the temperature.

Table 6: High Byte of the Temperature Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	T15	T14	T13	T12	T11	T10	T9	T8

Table 7: Low Byte of the Temperature Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	T7	T6	T5	T4	T3	T2	T1	T0

8.5.3 Configuration Register

The configuration register is a 16-bit read/write register used to store bits controlling the operating modes of the temperature sensor. Read/write operations are performed MSB first. Table 8 lists the format of the configuration register and the power-on default values.

Table 8: Configuration and Power-On Default Values

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD
	0	1	1	0	0	0	0	0
2	CR1	CR0	AL	EM	0	0	0	0
	1	0	1	0	0	0	0	0

Shutdown Mode (SD) Shutdown mode saves maximum power by turning off all device circuitry except for the serial interface, reducing the current consumption to typically less than $0.25\mu A$. When the SD bit=1, shutdown mode is enabled; the device shuts down once the current conversion is completed. When the SD bit=0, the device remains in continuous conversion state.

Thermostat Mode (TM) The thermostat mode bit indicates whether the device operates in comparator mode (TM=0) or interrupt mode (TM=1).

Polarity (POL) The polarity bit allows the user to adjust the polarity of the ALERT pin output. If the POL bit is set to 0, the ALERT pin is active low. When the POL bit is set to 1, the ALERT pin is active high and the state of the ALERT pin is inverted.

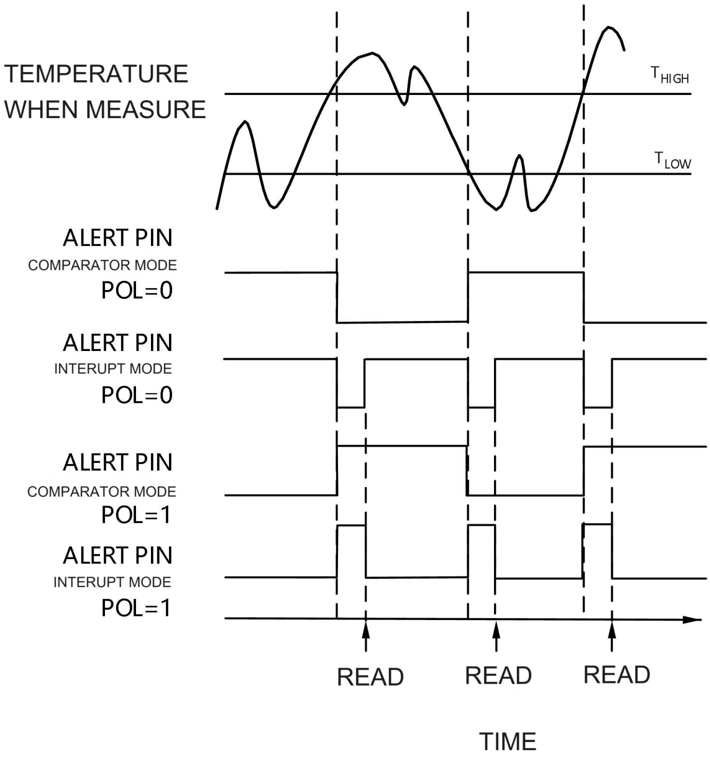


Figure 14: Output Transfer Function

Fault Queue (F1/F0) A fault condition exists when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} registers. Additionally, the fault queue can be used to program the number of fault conditions required to generate an alert. The fault queue is provided to prevent false alerts due to environmental noise. The fault queue requires consecutive fault measurements to trigger an alert. Table 9 lists the possible settings for the number of fault measurements that can trigger an alert condition in the device.

Table 9: KTP112 Series Fault Settings

F1	F0	Number of Consecutive Faults
0	0	1
0	1	2
1	0	4
1	1	6

One-Shot Mode (OS) When the device is in shutdown mode, writing a 1 to the OS bit starts a single temperature conversion. During conversion, the OS bit reads 0. After the single conversion is completed, the device returns to shutdown mode. For more information on one-shot conversion mode, see the One-Shot/Conversion Ready Mode (OS) section.

Alert (AL) The AL bit is a read-only function. Reading the AL bit provides information on the status of comparator mode. The state of the POL bit inverts the polarity of the data returned from the AL bit. When POL bit equals 0, the AL bit reads 1 until the temperature equals or exceeds T_{HIGH} for the programmed number of consecutive faults, causing the AL bit to read 0. The AL bit continues to read 0 until the temperature falls below T_{LOW} for the programmed number of consecutive faults, then reads 1 again. The state of the TM bit does not affect the state of the AL bit.

8.5.4 Upper and Lower Limit Registers

Temperature limits are stored in the T_{HIGH} and T_{LOW} registers in the same format as the temperature result and compared to the temperature result at each conversion. The result of the comparison drives the behavior of the ALERT pin, which operates as a comparator output or interrupt, set by the TM bit in the configuration register.

In comparator mode (TM=0), the ALERT pin becomes active when the temperature equals or exceeds the value in the T_{HIGH} register and remains active until the temperature falls below the value in the T_{LOW} register for the programmed number of consecutive faults.

In interrupt mode (TM=1), the ALERT pin is active when the temperature equals or exceeds the value in the T_{HIGH} register or falls below the value in the T_{LOW} register, seen in the Table 8. The ALERT pin is cleared when any register is read, or the device successfully responds to the SMBus alert response address. If the device is in shutdown mode, the ALERT pin is also cleared. The ALERT pin will be reactivated only if the temperature exceeds T_{HIGH} or falls below T_{LOW} for the programmed number of consecutive faults. This operation will also clear the status of the internal registers in the device, returning the device to comparator mode (TM=0). Both operation modes are shown in Figure 14. Tables 10 and Table 11 list the formats of the T_{HIGH} and T_{LOW} registers.

The power-on reset values of T_{HIGH} and T_{LOW} are:

- T_{HIGH} = $80°C$
- T_{LOW} = $75°C$

The data format for T_{HIGH} and T_{LOW} is the same as the temperature register.

Table 10: High Byte and Low Byte of the T_{HIGH} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H15	H14	H13	H12	H11	H10	H9	H8
2	H7	H6	H5	H4	H3	H2	H1	H0

Table 11: High Byte and Low Byte of the T_{LOW} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L15	L14	L13	L12	L11	L10	L9	L8
2	L7	L6	L5	L4	L3	L2	L1	L0

9 Applications and Implementation

9.1 Application Information

The KTP112 series is used to measure the PCB temperature at the device installation site. Programmable address options allow monitoring up to four locations on a single serial bus.

9.2 Typical Application Schematic

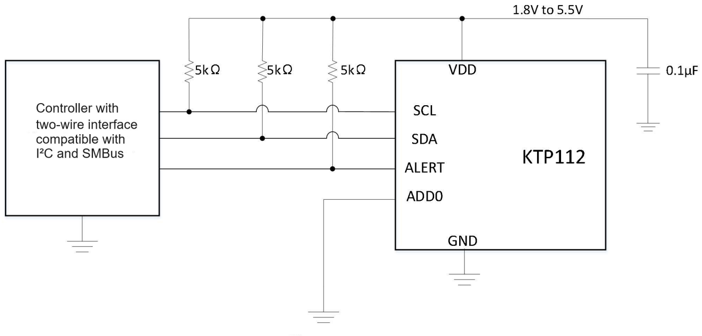


Figure 15: Typical Connection

The SCL, SDA, and Alert pins require pull-up resistors.

9.3 Design Requirements

The KTP112 series requires pull-up resistors on the SCL, SDA, and ALERT pins. The recommended value for the pull-up resistors is $5k\Omega$. In some applications, the pull-up resistors can be lower or higher than $5k\Omega$, but should not be less than 500Ω or exceed $10mA$ current on any of these pins. A $0.1\mu F$ bypass capacitor is recommended on the power supply, as shown in Figure 15. The SCL and SDA lines can be pulled up to a power supply equal to or higher than V+. To configure one of four different addresses on the bus, connect the ADD0 pin to GND, V+, SDA, or SCL.

9.4 Detailed Design Procedure

Place the device near the heat source that needs to be monitored to achieve good thermal coupling. This positioning ensures that temperature changes are captured within the shortest time interval. For applications requiring accurate air or surface temperature measurements, take care to isolate the package and leads from ambient air temperature. A thermally conductive adhesive helps achieve accurate surface temperature measurements.

The KTP112 series is a very low power device and generates very low noise on the power supply bus. Applying an RC filter to the V+ pin of the KTP112 series can further reduce any noise the device may propagate to other components. In Figure 16, R_F must be less than $5k\Omega$ and C_F must be greater than $10nF$.

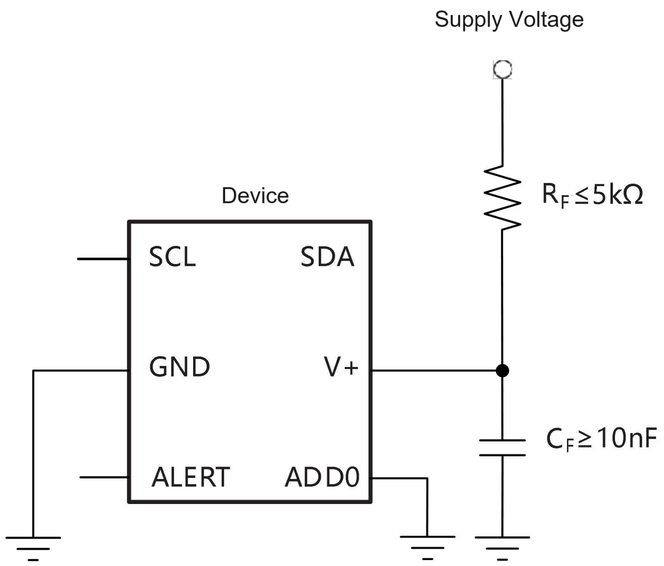


Figure 16: Noise Reduction Techniques

9.5 Application Curves

Figure 17 shows the step response of the KTP112 series immersed in a $100°C$ oil bath at room temperature ($26°C$). The time constant, or the time to reach 63% of the input step, is $3.1s$. The result of the time constant depends on the PCB on which the KTP112 series is mounted. In this test, the KTP112 series is soldered onto a two-layer PCB measuring 1.5 inches $\times$ 1.5 inches.

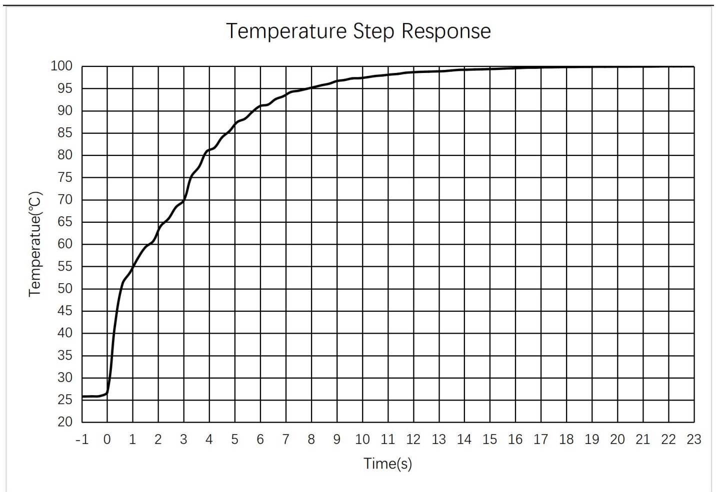


Figure 17: Temperature Step Response

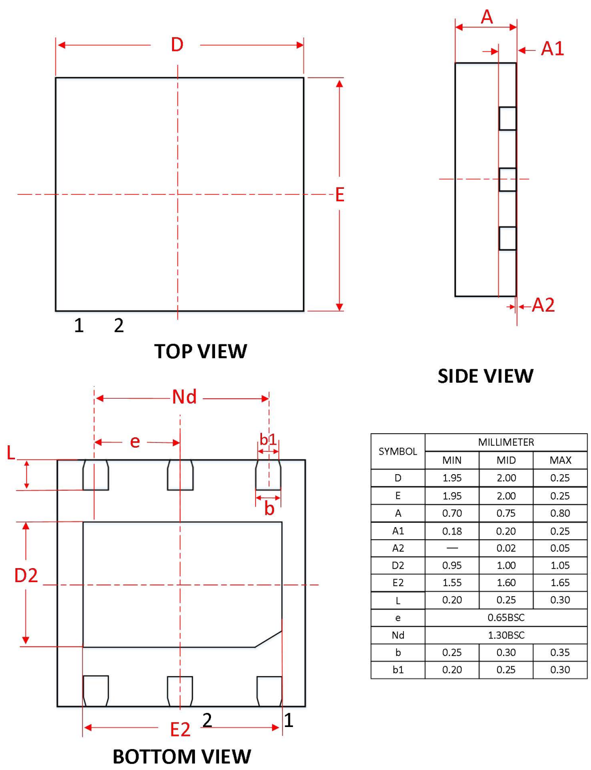
10 Power Supply Recommendations

The KTP112 series has a power supply range of $1.8V$ to $5.5V$. The device is optimized to operate at $3.3V$ but can accurately measure temperature across the entire power supply range. A power supply bypass capacitor is required for proper operation. Place this capacitor as close as possible to the power and ground pins of the device. The typical value of this power supply bypass capacitor is $0.1\mu F$. Applications with noisy or high impedance power supplies may require additional decoupling capacitors to suppress power supply noise.

11 Ordering Information

Part number	Package Type	MSL	Peak Temp (°C)	Operating Temp (°C)
KTP112-DZ6	DFN2×2-6L	Level-3	260	−40 to 125

12 Package Information



SYMBOL	MILLIMETER		
	MIN	MID	MAX
D	1.95	2.00	0.25
E	1.95	2.00	0.25
A	0.70	0.75	0.80
A1	0.18	0.20	0.25
A2	—	0.02	0.05
D2	0.95	1.00	1.05
E2	1.55	1.60	1.65
L	0.20	0.25	0.30
e	0.65BSC		
Nd	1.30BSC		
b	0.25	0.30	0.35
b1	0.20	0.25	0.30

Figure 18: DFN2×2-6L Package Dimensions